| Examiner-Initiated Interview Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/039,852 | SHIH ET AL. | |
| | Examiner | Art Unit | |
| | John P. Trimmings | 2138 | |

**All Participants:**

(1) *John P. Trimmings*.

(2) *Jiawei Huang*.

**Status of Application:** *Pending*

(3) _____.

(4) _____.

**Date of Interview:** *16 March 2006*

**Time:** *2:00 PM*

**Type of Interview:**
- ☒ Telephonic
- ☐ Video Conference
- ☐ Personal (Copy given to: ☐ Applicant ☐ Applicant's representative)

Exhibit Shown or Demonstrated: ☐ Yes ☒ No
If Yes, provide a brief description:

**Part I.**

Rejection(s) discussed:
*35 USC 102*

Claims discussed:
*1,2,6*

Prior art documents discussed:
*Crouch*

**Part II.**

SUBSTANCE OF INTERVIEW DESCRIBING THE GENERAL NATURE OF WHAT WAS DISCUSSED:

**Part III.**

☒ It is not necessary for applicant to provide a separate record of the substance of the interview, since the interview directly resulted in the allowance of the application. The examiner will provide a written summary of the substance of the interview in the Notice of Allowability.

☐ It is not necessary for applicant to provide a separate record of the substance of the interview, since the interview did not result in resolution of all issues. A brief summary by the examiner appears in Part II above.

(Examiner/SPE Signature)

(Applicant/Applicant's Representative Signature – if appropriate)

Continuation of Substance of Interview including description of the general nature of what was discussed: The examiner and applicant's representative,Jiawei Huang, agreed to claim amendments as follows:

Claim 1. (currently amended) A method of testing a chip that comprises an intellectual product circuit modules, the method comprising:
providing a test pattern;
sequentially enabling a common storage device to store the test pattern based on a plurality of different states; and after the test pattern is stored in the common storage device, selecting one of the intellectual product circuit modules according to the test pattern for testing by providing a test activating signal using a synchronous clock signal to the selected intellectual product circuit module in a next state, so that the selected intellectual product circuit module is operated and tested according to the test pattern from the common storage device.

Claim 2. (currently amended) A circuit for testing a chip that comprises an intellectual product circuit module, the circuit for testing the chip further comprising:
a common storage device coupled to the intellectual product circuit module; and
an input signal selector, coupled to the intellectual product circuit module and the common storage device, wherein the input signal selector receives a test pattern and sequentially enables the common storage device to store the test pattern based on a plurality of different states, after all of the test pattern is stored in the common storage device, in a next state the input selector further provides a test activating signal using a synchronous clock signal to the intellectual product circuit module so that the intellectual product circuit module is operated and tested according to outputs of the common storage device.

Claim 6. (currently amended) A circuit for testing a chip that comprises a plurality of intellectual product circuit modules, the circuit comprising:
an output selector, coupled to the intellectual product circuit modules to selectively output a test result from the intellectual product circuit modules;
a common storage device, coupled to the intellectual product circuit modules to output signals stored in the common storage device to the intellectual product circuit modules; and
an input signal selector, coupled to the intellectual product circuit modules, the output selector and the common storage device, the input signal selector for receiving a test pattern and sequentially enabling the common storage device to store the test pattern based on a plurality of different states of the input signal selector, and after all of the test pattern is stored in the common storage device, selecting one of the intellectual product circuit modules according to the test pattern for testing by providing a test activating signal using a synchronous clock signal to the selected one of the intellectual product circuit modules in a next state, so that the selected intellectual circuit module is operated and tested according to the output of the common storage device, and the input signal selector further controlling the output selector to selectively output the test results.

John P Trimmings
Examiner